CLAIMS

What is claimed is:

1. A semiconductor memory device comprising an array of memory cells arranged in rows and columns, wherein said array of memory cells comprises:

a plurality of non-intersecting STI regions isolating a plurality of columns of memory cells;

a source column implanted with n-type dopants isolated between an adjoining pair of said plurality of non-intersecting STI regions, said source column coupled to a plurality of source lines that are coupled to a plurality of source regions in said array of memory cells; and

a source contact coupled to said source column for providing electrical coupling with said plurality of source regions, said source contact located along a row of drain contacts that are coupled to drain regions of a row of memory cells.

2. The semiconductor memory device as described in claim 1, wherein locating said source contact along said row of drain contacts enables the straight formation of a word line intersecting said source column near said source contact.

3. The semiconductor memory device as described in claim 1, wherein said n-type dopants are taken from a group consisting of:

arsenic;

phosphorous; and

antimony.

4. The semiconductor memory device as described in claim 1, further comprising:

a second source contact strapped to said source column for reducing resistance in said plurality of source lines, and located along a second row of drain contacts that are coupled to drain regions of a second row of memory cells.

5. The semiconductor memory device as described in claim 1, wherein each of said plurality of source lines is a common source line.

6. The semiconductor memory device as described in claim 1, further comprising:

a second source column implanted with said n-type dopants and isolated between a second adjoining pair of said plurality of non-intersecting STI regions, said source column coupled to said plurality of common source lines, said source column located x columns of memory cells from said source column in claim 1 for reducing resistance in said plurality of common source lines.

7. The semiconductor memory device as described in claim 6, wherein said x is the number 16.

8. A non-volatile semiconductor memory device including an array of memory cells, said array of memory cells comprising:

a source column implanted with n-type dopants, said source column coupled to a plurality of common source lines that are coupled to a plurality of source regions of memory cells in said array of memory cells, said source column arranged perpendicular to each of said plurality of common source lines; and

a source contact coupled to said source column for providing electrical coupling with said plurality of source regions, said source contact located along a row of drain contacts coupled to drain regions of a row of memory cells that are arranged perpendicular to said source column.

9. The non-volatile semiconductor memory device as described in claim 8, further comprising:

a plurality of word lines coupled to control gate regions of memory cells in said array of memory cells, said plurality of word lines exhibiting straightness at intersections with said source column adjacent to said source contact.

10. The non-volatile semiconductor memory device as described in claim 8, further comprising:

a plurality of STI regions arranged in non-intersecting columns on a silicon substrate, said plurality of STI regions isolating columns of memory cells in said array of memory cells, and isolating said source column.

11. The non-volatile semiconductor memory device as described in claim 8, wherein said source contact is of similar dimension as each of said row of drain contacts.

12. The semiconductor memory device as described in claim 8, wherein memory cells in said array of memory cells are arranged in a NOR configuration.

13. The semiconductor memory device as described in claim 8, wherein at least one of said array of memory cells is a flash memory cell comprising:

a tunnel oxide layer formed on a semiconductor substrate between source and drain regions;

a floating gate formed on said tunnel oxide layer;

a multi-level insulating layer formed on said floating gate; and

a control gate formed on said insulating layer.

14. The semiconductor memory device as described in claim 8, further comprising

a second source contact strapped to said source column for reducing resistance in said plurality of common source lines, and located along a second row of drain contacts that are coupled to drain regions of a second row of memory cells.

15. The semiconductor memory device as described in claim 8, further comprising:

a second source column implanted with said n-type dopants, said source column coupled to said plurality of common source lines, said source column located x columns of memory cells from said source column in claim 1 for reducing resistance in said plurality of common source lines.

16. A method of forming a source line contact in a non-volatile memory comprising:

forming a source column in an array of memory cells, said array of memory cells comprising a plurality of memory cells arranged in a matrix of rows and columns, said array of memory cells including at least one row of drain contacts for accessing drain regions in associated rows of memory cells in said array of memory cells;

coupling a plurality of source contacts to said source column, each of said plurality of source contacts located in-line with an associated row of drain contacts; and

coupling said source column to a plurality of source lines that are perpendicular to said source column, and for providing electrical coupling to a plurality of source regions in said array of memory cells, said plurality of source lines coupled to said plurality of source regions.

17. The method as described in claim 16, further comprising:

forming a plurality of word lines in said array of memory cells perpendicular to said source column, and each of said plurality of word lines not requiring any bending to accommodate each of said plurality of source contacts.

18. The method as described in claim 16, further comprising:

implanting n-type dopants to form said source column, said n-type dopants also implanted under a plurality of word lines in said array of memory cells.

19. The method as described in claim 18, further comprising:

implanting said n-type dopants after formation of a plurality of STI columns, said plurality of STI columns isolating columns of memory cells and said source column in said array of memory cells.

20. The method as described in claim 18, further comprising:

implanting said n-type dopants before formation of said plurality of word lines.

21. The method as described in claim 18, further comprising:

before said step of implanting said n-type dopants in claim 18, masking said source column with a photoresist layer.

22. The method as described in claim 16, wherein at least one memory cell of said array of memory cells is a flash memory cell.

23. The method as described in claim 16, further comprising:

arranging said array of memory cells in a NOR type configuration.

24. The method as described in claim 16, wherein each of said plurality of source lines is a common source line.

25. A method of forming a source line contact in an array of memory cells comprising:

a) forming a plurality of shallow trench isolation (STI) regions in non-intersecting columns in a silicon substrate, said plurality of STI regions isolating a plurality of columns of silicon in said silicon substrate;

b) after said step a), implanting n-type dopants in at least one of said plurality of columns of silicon to form a source column;

c) forming a plurality of common source lines across said array of memory cells, said plurality of common source lines perpendicular to said source column;

d) coupling said plurality of common source lines to source regions in said array of memory cells;

e) permanently coupling said plurality of common source lines to said source column; and

f) forming a source contact along a row of drain contacts associated with a row of memory cells perpendicular to said source column, said source contact coupled to said source column.

26. The method as described in claim 25, further comprising:

before b), masking said source column to isolate said source column.

27. The method as described in claim 25, further comprising:

after step b), forming a plurality of tunnel oxide layers on a semiconductor substrate between respective source and drain regions;

forming a plurality of floating gates formed on said plurality of tunnel oxide layers;

forming a plurality of interpoly dielectric layers on said plurality of floating gate layers; and

forming a plurality of control gates on said plurality of interpoly dielectric layers.

28. The method as described in claim 25, further comprising:

before c), implanting n-type dopants in said plurality of columns of silicon to form source and drain regions in memory cells of said array of memory cells;

29. The method as described in claim 25, further comprising:

forming a plurality of word lines that are non-intersecting across said array of memory cells, said plurality of word lines coupled to a plurality of control gates in said array of memory cells, said plurality of word lines exhibiting straightness at intersections with said source column adjacent to said source contact.